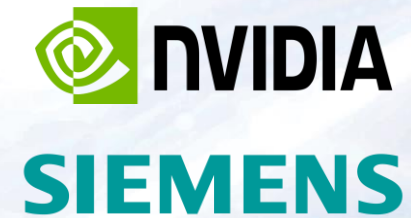




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# AI-Powered High-Sigma Automated Full Library Verification Methodology for Standard Cells



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# NVIDIA's Digital IP Group Mission and Use-cases

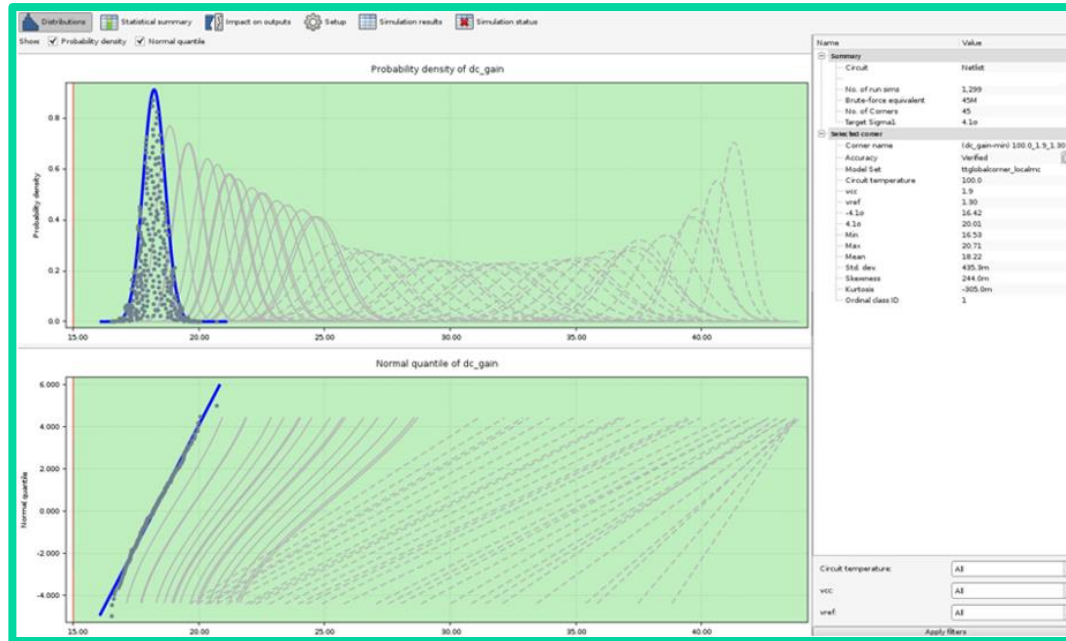
- **NVIDIA's Digital IP group offers in-house highly competitive designs, including:**
  - Full Standard Cell Library
  - Custom ROMs
  - SRAM Compilers
  - Other IP designs
- **The group's mission is to deliver first-time working silicon IPs at speed-of-light with best-in-class performance, power and area, using robust and adaptive methodologies**
- **One of NVIDIA's main use-cases is to verify our standard cell libraries**
  - Example: Library has 100 cells; 2 threshold voltages ( $V_t$ ) and 5 PVT corners per cell
    - 1,000 total combinations

# Nvidia's Problem Statement

- Goal
  - Verify yield of each combination as quickly as possible
  - Need to discern between **A**, **B**, and **C**:
    - Where:  $A < 5.5\sigma < B < 6.5\sigma < C$
    - If **B**, needs precise brute-force accurate yield
- Challenging Requirements
  - Automatic
    - Manual setup for each cell combination is tedious and time consuming
  - Brute-force accurate
    - Rare failures cannot be missed, but  $6.5\sigma$  verification requires 100+ billion simulations
  - Sign-off in production runtimes
    - Solution needs to be magnitudes faster than brute-force simulation

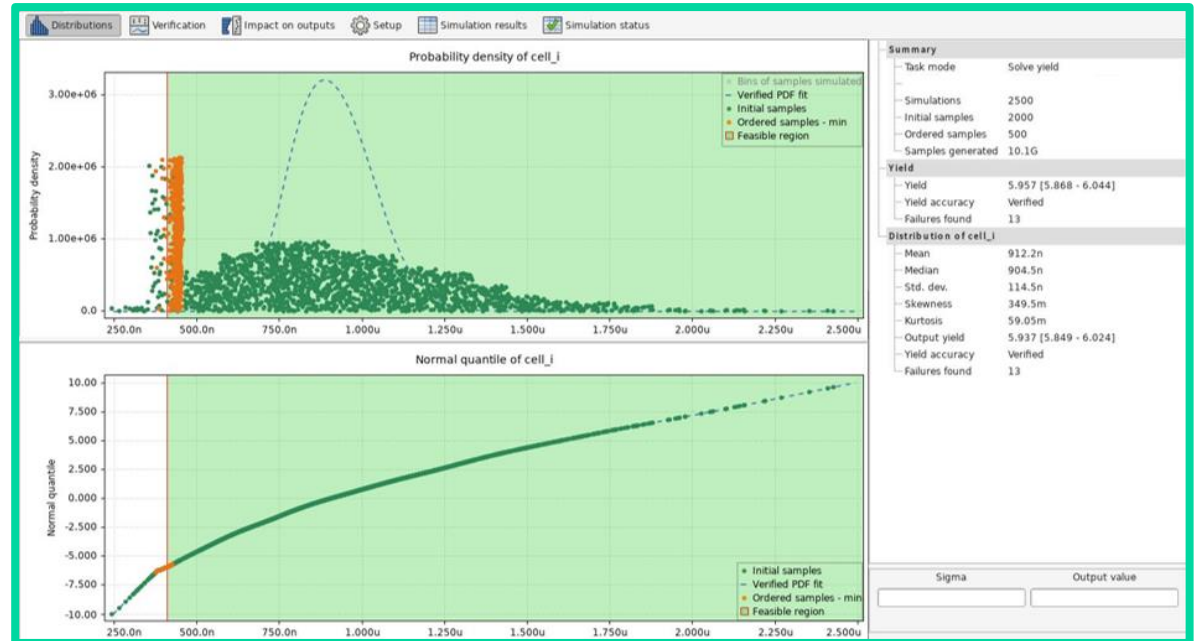
# NVIDIA Leveraging Solido Design Environment for Standard Cell Verification

## Solido PVTMC Verifier and High-Sigma Verifier



### Solido PVTMC Verifier

- Solve yield mode can be used to verify yield with good accuracy in reduced simulations
- Quickly determines if yield is very high or low
- Finds rare outliers other methods can't



### Solido High-Sigma Verifier

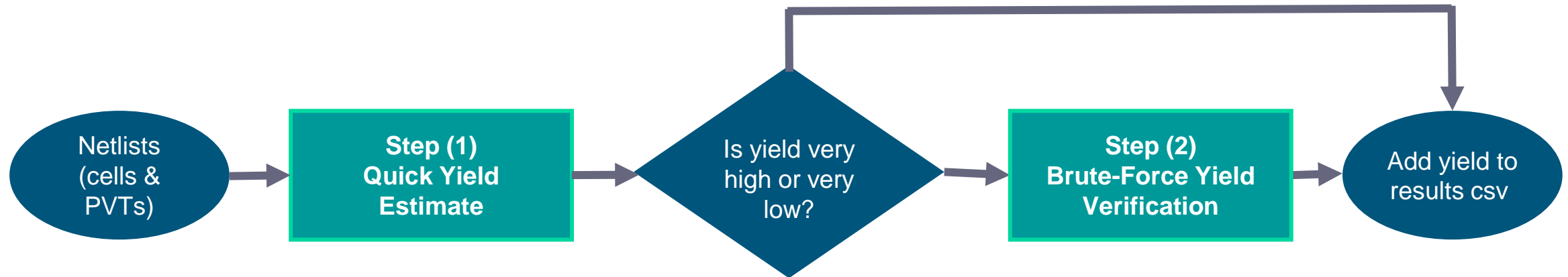
- Verifiable brute-force accurate high-sigma verification
- Precise yield verified in only 1,000's of simulations
- 1,000x - 1,000,000,000x+ faster than brute-force, while maintaining SPICE accuracy

# NVIDIA's AI-Powered Flow with Solido for Standard Cell Verification

## 30x faster than best alternative with same brute-force accuracy

Solido Library Yield Solver flow, **AI-powered automated** methodology for detecting and verifying the yield of all cells

1. Solido PVTMC Verifier – Initial step to produce quick yield estimate
  - User specifies which cells move forward to second step (e.g., between  $5.5\sigma$  –  $6.5\sigma$ )
2. Solido High-Sigma Verifier – (If necessary) Secondary step to verify precise brute-force accurate yield

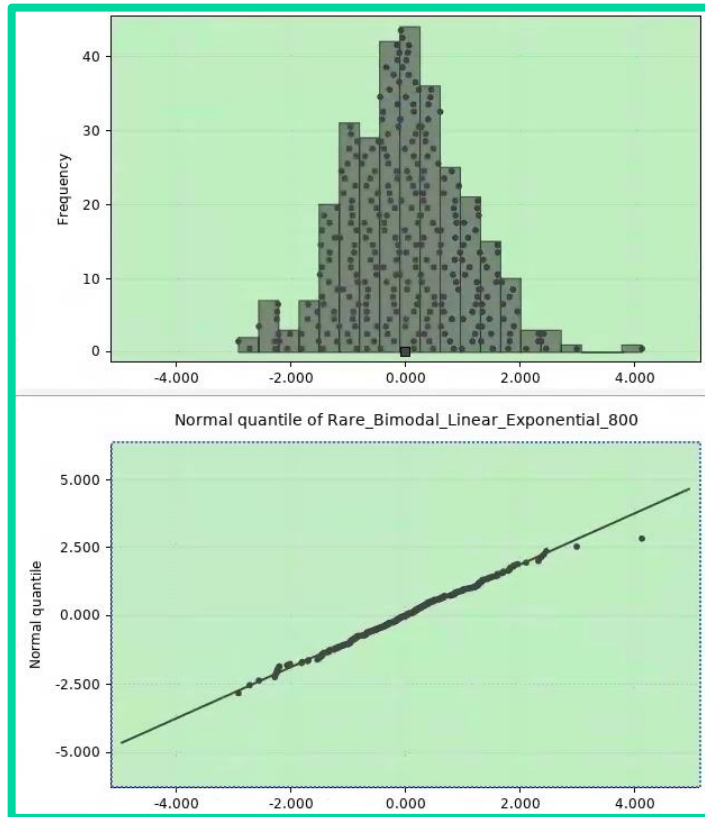


Solido Library Solver flow provides **30x speedup** compared to best alternative (HSV-only flow)  
Quickly verifies cells and determines cells out of user-defined yield,  
and runs cells requiring higher precision for brute-force accuracy

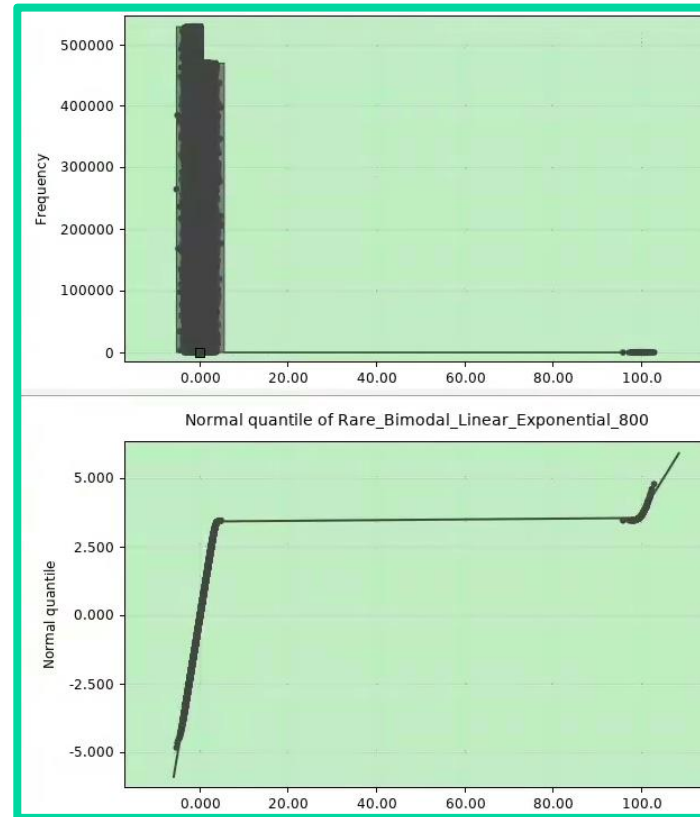
# NVIDIA's Standard Cell Verification Challenge

## High-sigma run time and coverage

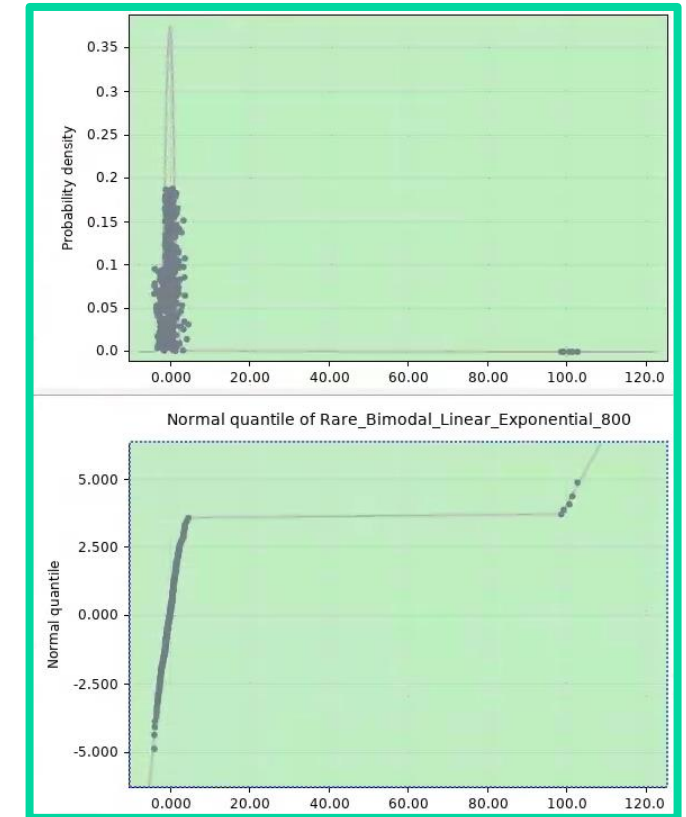
- Yield verification requires ability to find real failures at high sigma



Traditional MC (300 MC); Extrapolation would be required to reach high sigma



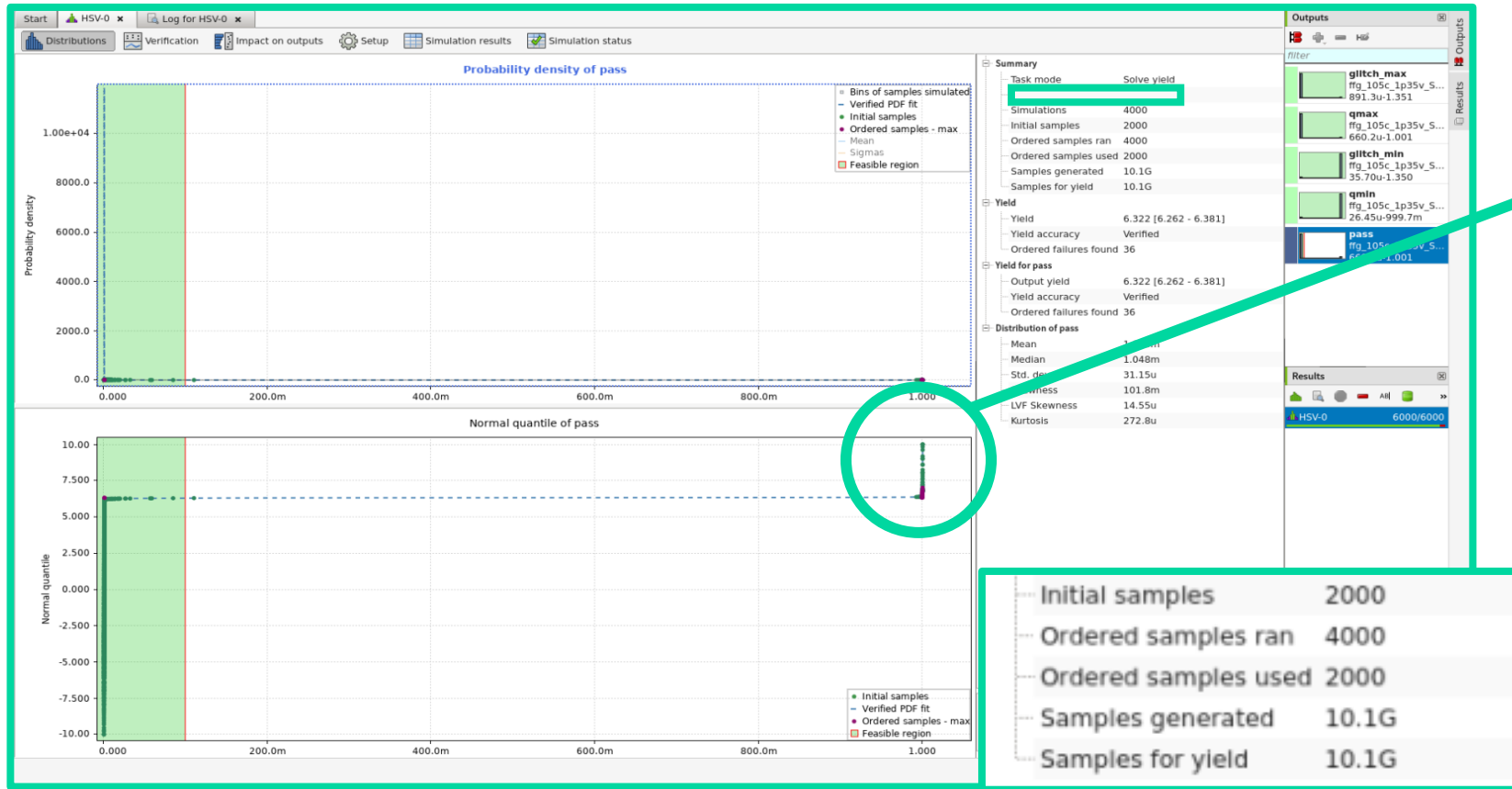
Brute-force (1M MC); Extrapolation wouldn't find these failures



Solido (300 MC); Able to see rare failures in fewer simulations

# Solido High-Sigma Verifier Able to Accurately Identify Bimodality Failure

## 6.3 sigma verification, orders of magnitude faster than brute-force



### Latch-based D flip flop circuit

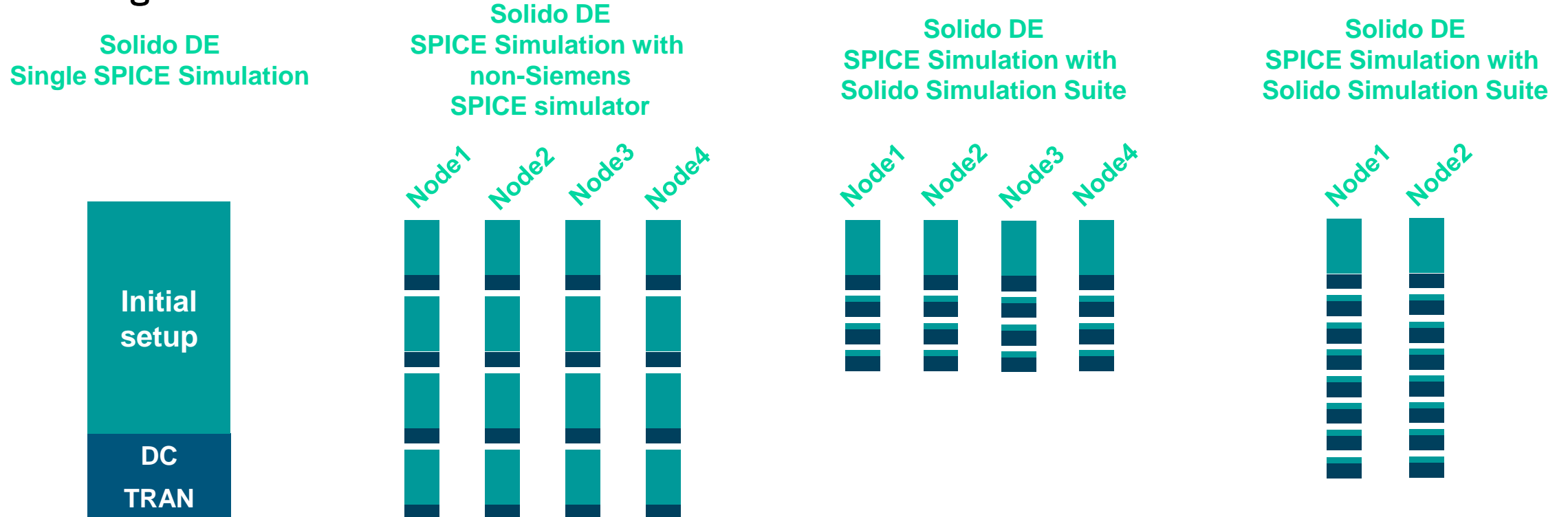
- Bimodality failure occurrence
- Solido High-Sigma Verifier used only 4,000 simulations
  - 1,683,000x faster than brute force simulation
- Yield at this cell / PVT is precisely verified to 6.322σ

# Differentiated SPICE simulator integration with Solido Simulation Suite

## Provides **2.5x additional speedup**

- Solido Simulation Suite integration with Solido DE significantly reduces initial simulation setup overhead
- Resulting in speedups in statistical simulations for memory and standard cell applications
- Provides **2.5x additional speedup** for circuits with large front-end setup time and small simulation time

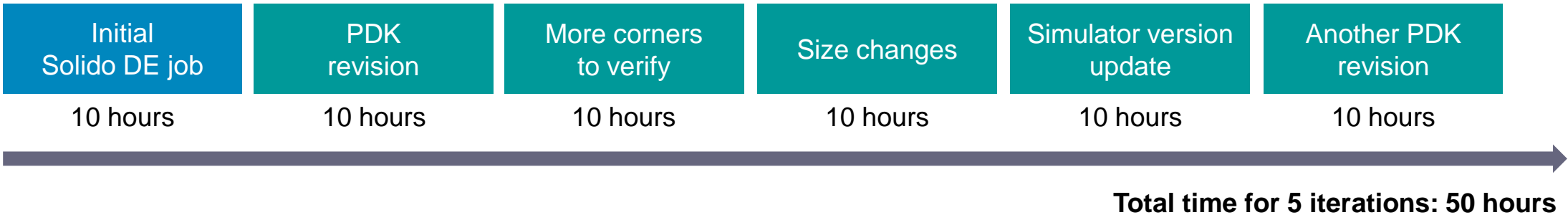
### How the integration works:



# Solido Additive Learning Technology Introduction

## Transitioning from individual verification jobs to iterations

### Traditional workflow:



### Solido iterative workflow:

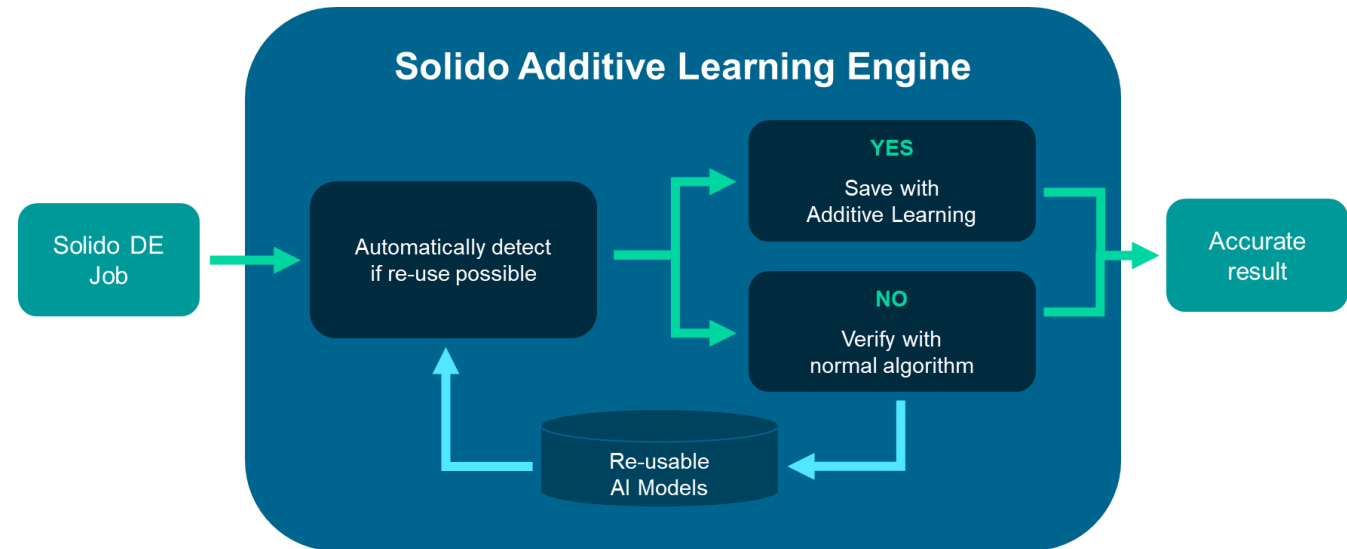


# Solido Additive Learning

## Delivers accurate results every time, automatically

Solido Additive Learning for iterative jobs

- Re-uses AI models from previous runs to significantly save simulations
  - On iterative runs: PDK revisions, sizing changes, tool version updates, adding more corners, etc.
- Fast
  - Faster for iterative jobs
- Accurate
  - Equivalent to full verification job
- Automatic
  - AI constantly tracks and makes decisions



# A Solido AI-powered NVIDIA Methodology

Providing cumulative **120x Speedup** compared to best alternative flow

To achieve 6-sigma verification across full standard cell library:

100 standard cells \* 2 Vts \* 5 PVTs = 1,000 combination

Library Methodology	Runtime
Brute-force MC	~10.1T * 1,000 Runtime: not feasible
Solido Library Yield Solver	<b>30x faster</b> than best alternative (HSV-only flow)
Solido Library Yield Solver with Analog FastSPICE (AFS)	2.5x Cumulative (30x*2.5x)= <b>75x</b> faster than best alternative
Solido Library Yield Solver with AFS and with Additive Learning technology (early access)	1.6x Cumulative (75x*1.6x)= <b>120x</b> faster than best alternative

# Summary

- High-Sigma verification for standard cells is complex and time-consuming
- Brute-force Monte Carlo and SPICE-accurate methods for high sigma verification is costly and not feasible
- Non-gaussian distribution circuits is an additional challenge layer
- Solido's solution accomplishes all requirements
  - Automatic
    - Automated flow that verifies all cell combinations in a simple to use method
  - Brute-force accurate
    - Solido's high-sigma technology ensures perfect SPICE accuracy where it matters and catches any rare failures
  - Sign-off in production runtimes
    - Solution is magnitudes faster than brute-force simulation
- Results
  - Showing cumulative **120x speedup** for full flow compared to best alternative methodology
  - Within verification cycle and across verification cycles with incremental changes